Evaluation Board Analog Output Functions and Characteristics

Application Note | July 2002 | AN1023

Introduction

The ISL5239 Evaluation Board includes the circuit provisions to convert the baseband digital I and Q outputs of the ISL5239 to differential analog I and Q output signals that are suitable to drive an analog quadrature modulator (AQM) circuit for direct up-conversion to RF.

This Application Note describes the performance characteristics of the DAC and analog output stages of the Evaluation Board. It also provides information for adjusting the Evaluation Board for different analog interfacing requirements, and provides instructions and examples for changing the analog I and Q low-pass filter bandwidths. The Application Note includes performance measurements for a typical application.

The Evaluation Board is shipped with a set of low-pass filters that have 3 dB bandwidth of approximately 42 MHz. When corrected with the digital correction filters of the ISL5239, an ideally flat response of greater than 80 MHz can be obtained. In some linearization applications, a wider pre-distortion signal bandwidth may be desired. The Application Note provides two alternate designs that can be simply implemented on the Board with component value changes only. The alternate designs achieve a 3 dB bandwidth of approximately 53 MHz, thus providing a full 100 MHz of flat RF passband pre-distortion signal bandwidth.

Overview of DAC and Analog Output Circuits

The analog output circuits feature the Intersil ISL5929 14-bit Dual-DAC and two fully differential DC-coupled low-pass filter and buffer amplifier sections for I and Q outputs. The outputs are suitable for directly driving the inputs of contemporary analog quadrature modulator RFICs such as the Sirenza STQ-2016 with performance levels limited only by the RFIC dynamic range. DC-coupling allows the ISL5239 to digitally control the DC offsets and balance of the baseband modulator channels to achieve nearly perfect carrier suppression.

The combination of analog output circuits and digital processing capabilities of the ISL5239 allow the following output signal parameters to be adjusted with high precision:

- Output signal level (independently adjustable for I and Q)
- DC-offset (independent for I and Q)
- DC common mode output voltage
- Quadrature phase relationship of I and Q
- Quadrature gain relationship of I and Q
- Quadrature group delay relationship of I and Q
- Full-scale digital saturation output voltage level
- Common I and Q frequency response
- Differential I and Q frequency response

Figure 1 shows a simplified circuit schematic of one analog I or Q output channel of the Evaluation Board.

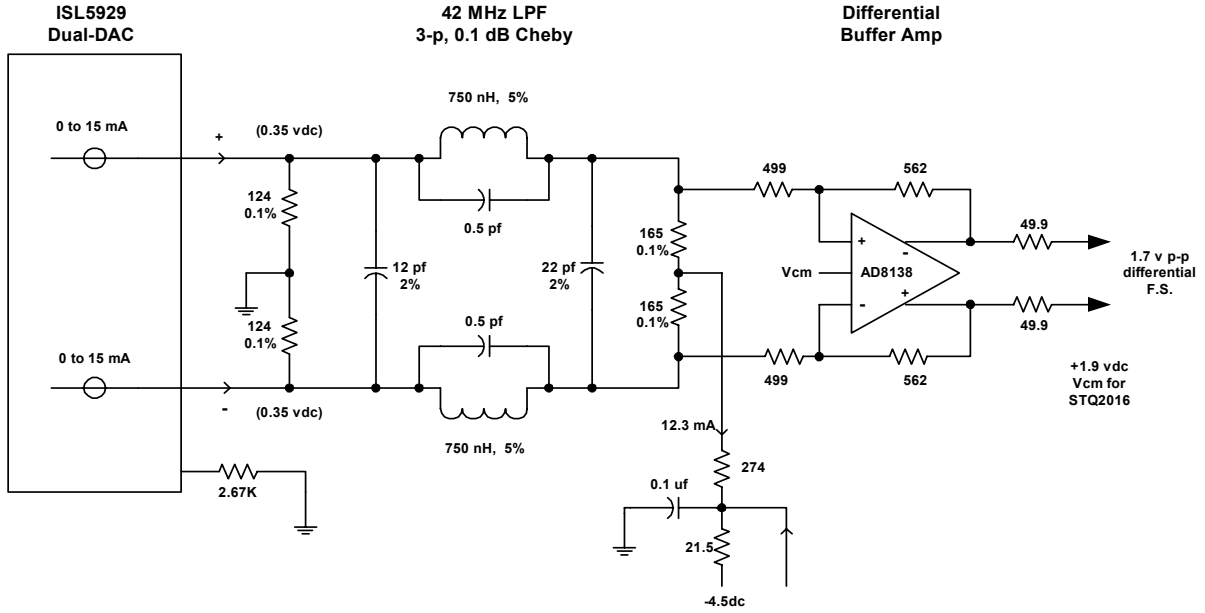

FIGURE 1. SIMPLIFIED SCHEMATIC OF ONE ANALOG OUTPUT CHANNEL

The DAC sampling rate for the ISL5239 Eval Board is 125 MHz. The 2.67K resistor sets the full scale DAC output currents to approximately 15 mA.

The differential outputs of the DAC current sources drive a fully-differential symmetrically- terminated 3-pole elliptical low-pass filter. The filter characteristic is approximated by a 3-pole, 0.1 dB passband ripple Chebychev response with 3 dB corner at 42 MHz and a transmission zero at about 190 MHz.

The filter output is buffered by a fully differential amplifier (AD8138) to provide a well controlled resistive output source impedance to the AQM through 50Ω lines. The analog outputs are intended to connect directly to high-impedance AQM inputs through short low-capacitance coax lines. This configuration permits full output swings into the AQM with minimal high frequency distortion due to the buffer amp drivers and loading.

A resistor divider bias network is shared between the two channels in order to set the common mode DC operating levels of the filters to the middle of the DAC output compliance range (approximately 0.35 vdc).

A Common Mode Output Voltage potentiometer, R62 on the Eval Board schematic, is used to set the output DC common mode voltage of both I and Q channels to a level between 0.0 vdc and 2.5 vdc. The output common mode voltage is set by the AD8138 based on this adjustable control voltage. For the Sirenza STQ-2016 AQM, this voltage should be set for approximately 1.90 vdc.

With the DAC currents set for 15 mA, the full scale output at the analog I and Q outputs is approximately 1.75 v p-p. This level can be adjusted up or down by changing the DAC current setting resistor, R9 on the Eval Board schematic, and making appropriate adjustments to the filter biasing current in order to maintain a filter bias voltage that is roughly centered within the DAC output compliance range.

Analog Filter Characteristics

Version 1: 42 MHz Bandwidth (shipped with Eval Board)

The baseline analog low-pass filters which come with the ISL5239 Eval Board have a 3 dB bandwidth of approximately 42 MHz, as shown in the simulated response plots below.

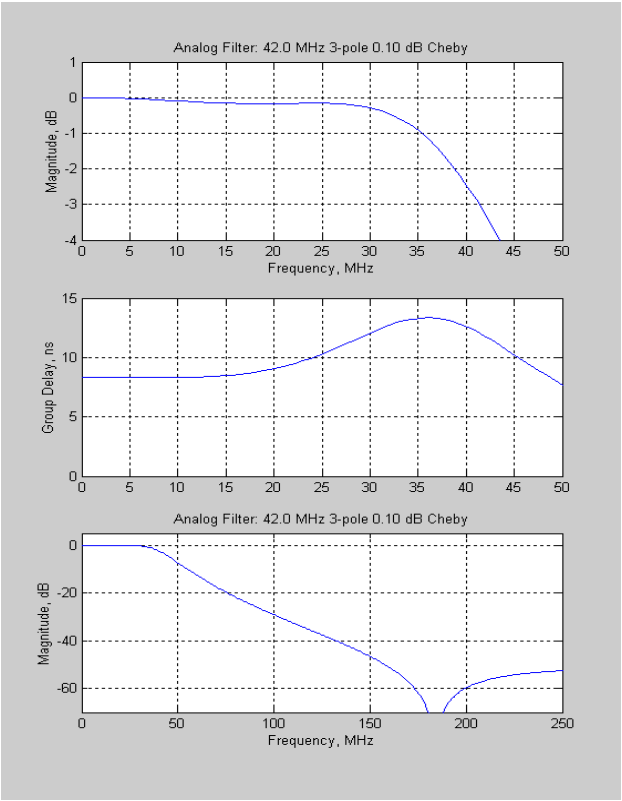

FIGURE 2. RESPONSE PLOTS OF THE 42.0 MHz LOW PASS FILTER

The filters and buffer amp together provide about 40 dB of attenuation of the DAC output signal spectrum at the sampling rate of 125 MHz. A transmission zero occurs at approximately 180 MHz based on the total equivalent parallel capacitance seen across the inductors. This zero has the effect of introducing a slight tilt to the passband characteristic of the normal Chebychev filter and produces a typical 3-pole elliptical response. Introduction of this zero ensures several more dB of attenuation at 125 MHz than otherwise.

Precision components are used in the critical filter elements to improve I and Q matching and response consistency.

The filter circuit is based on the standard normalized 3-pole 0.1 dB passband ripple Chebychev filter model, shown below.

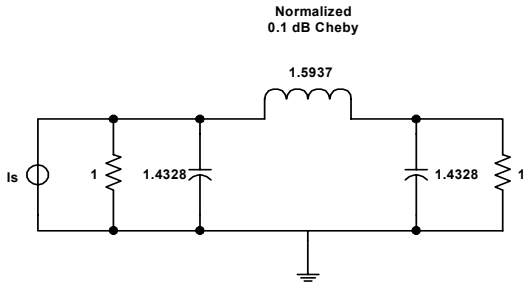

FIGURE 3. NORMALIZED 0.1 dB CHEBYCHEV FILTER

This model is a single-ended symmetrically terminated filter normalized to an impedance of 1Ω and 3 dB frequency of 1 radian per second. When scaled to 124Ω and a 3 dB frequency of 42 MHz, the element values become those shown in the following figure.

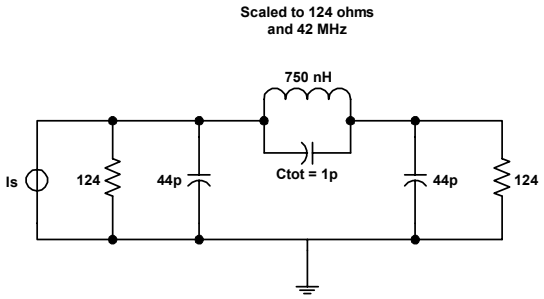

FIGURE 4. FILTER MODEL SCALED TO 124Ω AND 42 MHz BANDWIDTH

The addition of a parallel capacitance across the inductor introduces a transmission zero. This capacitance is partly due to the parasitic capacitance of a practical inductor which limits its self-resonant frequency. We add a small capacitor to set the zero frequency at approximately 190 MHz.

In realizing the final circuit element values, several other factors need to be included. In the differential form of this filter, the shunt capacitor values are scaled by 1/2 since capacitors are effectively in series. In addition, the output capacitance of the DAC and the parasitic pad and trace capacitances at the DAC output need to be included in the total capacitance seen at the input nodes of the filter. The assumptions used in the Evaluation Board design are as follows:

- DAC output capacitance: 11pf
- Pad and trace capacitances: 6pf

These filter model assumptions then produce the final circuit component values shown in the simplified Evaluation Board schematic given above.

Note that the effective differential voltage gain from the DAC output to the final buffered output is approximately one for frequencies within the passband of the filter. The balanced differential nature of the filter facilitates excellent rejection of clock and digital switching noise from the Eval Board digital circuits.

Version 2

53 MHz BW (Suggested Modification)

For full bandwidth baseband pre-distortion linearization applications or digital IF upconversion applications, a wider analog filter bandwidth is recommended. This section explains simple design modifications and component value substitutions on the Evaluation Board that will increase the analog filter bandwidths to approximately 53 MHz.

However, since the order of the filter remains 3-pole, the wider bandwidth filters will provide less attenuation at the sampling frequency of 125 MHz. The 125 MHz filter attenuation decreases from approximately 40 dB to 30 dB.

The 53 MHz filter is based on the normalized 3-pole 0.01 dB passband ripple Chebychev filter model given below.

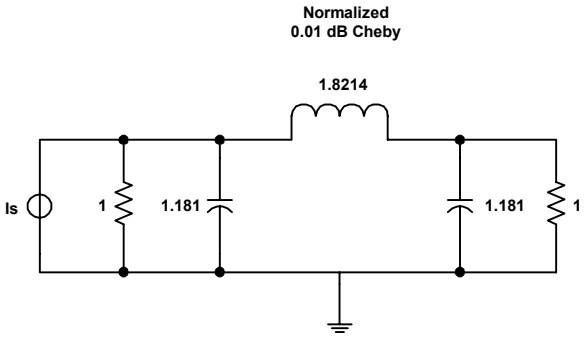

FIGURE 5. NORMALIZED 0.01 dB CHEBYSHEV FILTER

The frequency (bandwidth) of an R-L-C filter of this type can be scaled by scaling any two or more of the Rs, Ls, or Cs element values. With the goal of using standard available inductor values, we provide two alternative filter versions, each with 3 dB bandwidth of approximately 53 MHz.

Version 2 analog filter keeps the filter impedance at 124Ω, and uses a standard 680 nH inductor value. This single ended model is shown below. The alternative Version 3 analog filter uses a standard 750 nH inductor value and scales the filter impedance to 137Ω.

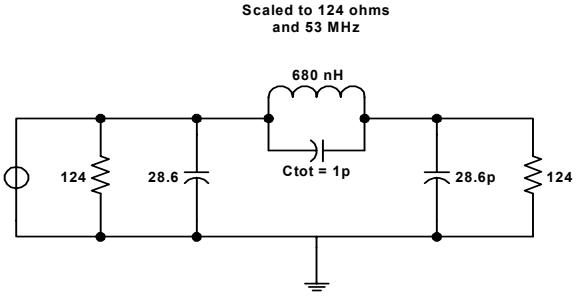

FIGURE 6. FILTER MODEL SCALED TO 124Ω AND 53.0 MHz BANDWIDTH

The simulated characteristics of the 53 MHz bandwidth filter designs are shown in the plots below. Again, the transmission zero introduces a slight tilt in the normally flat 0.01 dB Chebychev passband, but adds several more dB attenuation at 125 MHz than otherwise. The non-flatness is of little consequence and can be easily removed by using the ISL5239 digital correction filters.

The final filter element value changes for filter Version 2 are shown in the modified simplified schematic below.

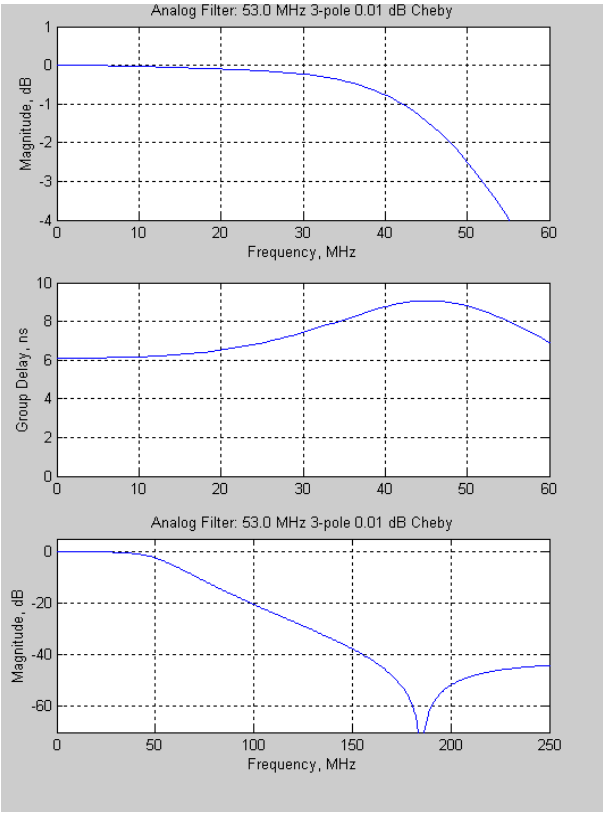

FIGURE 7. RESPONSE PLOTS OF 53.0 MHz LOW PASS FILTER

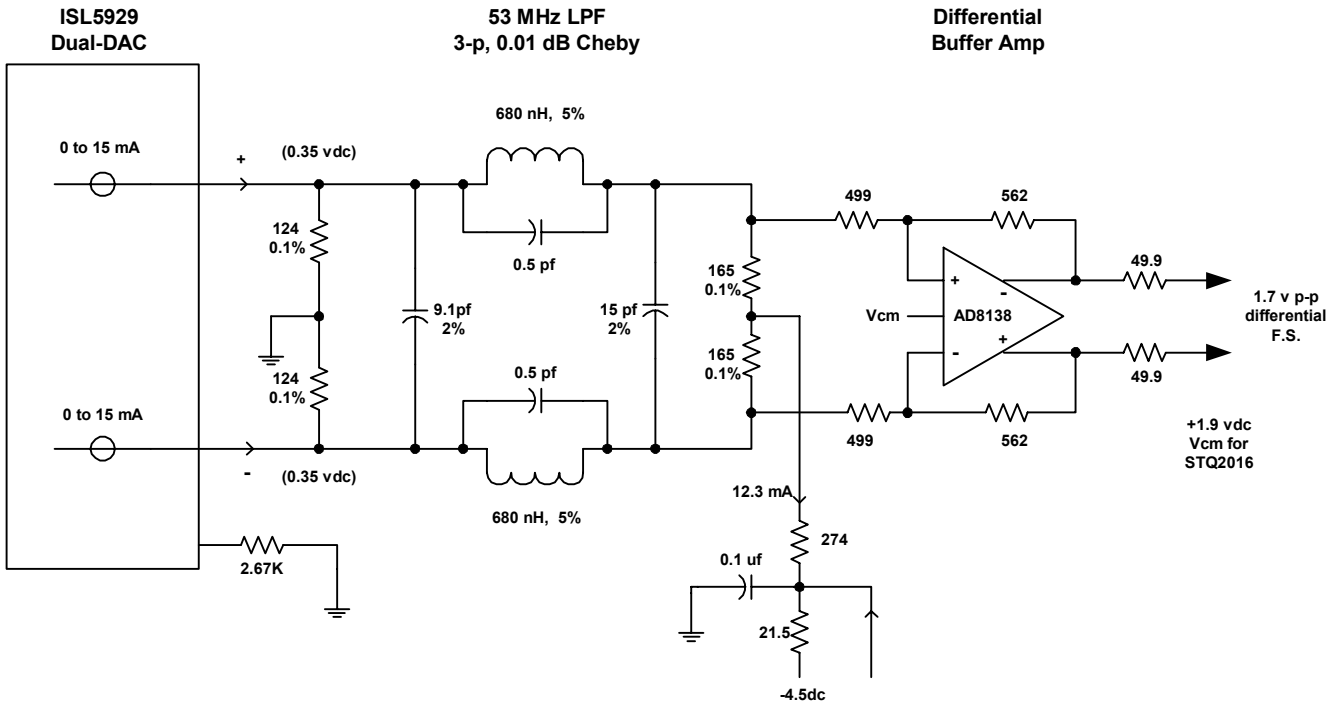

FIGURE 8. SIMPLIFIED SCHEMATIC WITH VERSION 2 FILTER

To implement the version-2 53MHz bandwidth filters on the ISL5239 Evaluation Board, the following L and C component substitutions should be made:

TABLE 1. L AND C COMPONENT SUBSTITUTIONS

	WAS	IS
L1, L2, L3, L4	750 nH, 5%	680 nH, 5%
C95, C105	12.0 pf, 2%	9.1 pf, 5%
C96, C106	22 pf, 2%	15 pf, 2%

The substitute inductors should be of the same characteristic family as specified in the original ISL5239 Evaluation Board BOM.

Version 3

53 MHz BW (Alternative Modification)

The alternative filter is based on scaling R's and A's only. The scaled model is as follows:

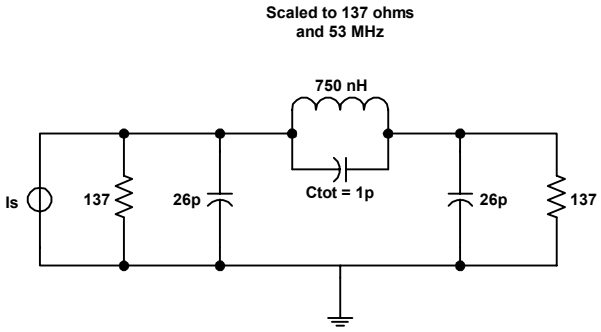

FIGURE 9. FILTER MODEL SCALED TO 53.0 MHz AND 137Ω

The final filter element value changes for filter version 2 are shown in the modified simplified schematic below.

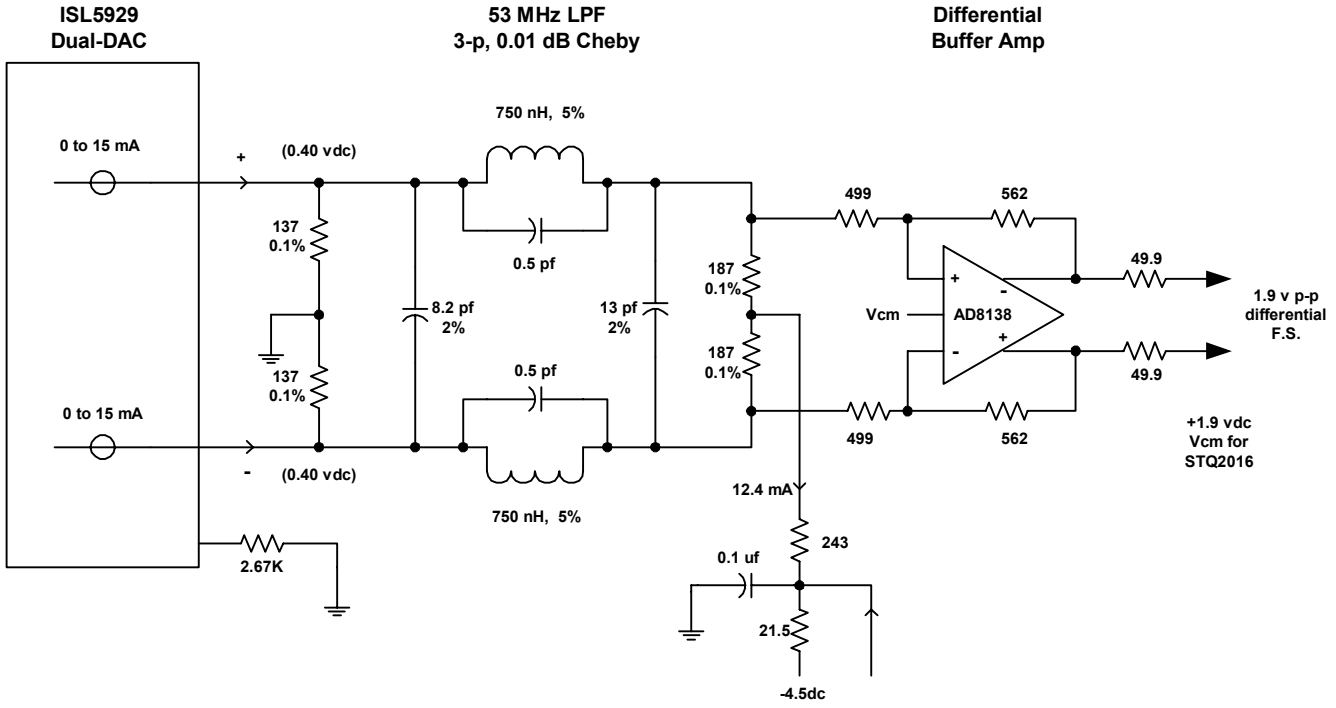

FIGURE 10. SIMPLIFIED SCHEMATIC WITH VERSION 3 FILTER

TABLE 2. L AND C COMPONENT SUBSTITUTIONS

	WAS	IS
R50, R54, R69, R73	124Ωs, 0.1%	137Ω, 0.1%
R51, R55, R70, R74	165Ω, 0.1%	187Ω, 0.1%
C95, C105	12.0 pf, 2%	8.2 pf, 5%
C96, C106	22 pf, 2%	13 pf, 2%
R61, R65	274Ω, 1%	243Ω, 1%

To implement the version-3 53MHz bandwidth filters on the ISL5239 Evaluation Board, the following R and C component substitutions should be made:

Versions 2 and 3 of the filter should result in nearly the same frequency response characteristic as shown above. Version 3 has slightly larger output level due to the increased filter impedance.

Output Adjustment and Loading Considerations

The analog output path design allows flexibility for setting the common mode DC output level and the peak differential analog output levels that correspond to full scale signals from the DACs. To obtain full performance, care must be exercised in the impedance loading at the outputs.

The circuits are designed to drive a relatively high impedance load over short, matched 50Ω lines between the Evaluation Board and an analog AQM circuit. The outputs may also be loaded with 50Ω, but with reduced distortion performance and a 6 dB decrease in output level. The differential outputs may be loaded unsymmetrically without unbalancing the filter impedances.

Please become familiar with the following recommendations:

Common Mode DC Output Voltages

Before operating the ISL5239 Evaluation Board, the Common Mode DC output voltages of the I and Q output pairs should be set appropriately for the application.

Since the DC output characteristics are directly controlled by the ISL5239 IC, it is recommended that the ISL5239 be initialized to have zero digital DC offset and zero digital DC output level on both I and Q channels before making set-up adjustments. When initialized, the differential DC levels of both the I and Q outputs should typically be less than 3 mV.

Potentiometer R62 should be adjusted to set the common mode DC levels of the I and Q outputs to a desired voltage between 0.0 vdc and 2.5 vdc.

The I and Q outputs will normally not be sourcing significant DC current when driving high resistance loads such as the inputs of an AQM device.

However, when any of the outputs is terminated in a lower impedance load such as 50Ω, then the common mode DC voltage may cause significant DC current to be sourced to the load. This will reduce the distortion performance of the AD8138 differential driver. Therefore, when observing the I or Q output signals with a 50Ω instrument, it is recommended that the common mode DC output voltage be set to zero.

The differential output drivers can support an unbalanced load (e.g. 50Ω load on one side only) without a significant change in performance characteristics. The distortion contribution of the differential output buffer amp will increase slightly at higher frequencies when loaded with 50Ω loads. Thus, for best distortion performance, it is recommended that the load impedance be divided down so as to remain greater than about 200Ω.

When driving an AQM device such as the Sirenza STQ-2016, the common mode DC output level should be set as recommended by the AQM vendor. This voltage will effect the distortion performance of the AQM and may need to be tuned to a level that minimizes operating distortion. For the STQ-2016, the optimum common mode levels are approximately 1.90 vdc to 1.95 vdc.

Full-Scale Output Signal Voltage

As shown in the schematic of Figure 2-1, the ISL5929 DAC output currents are set for approximately 15 mA. The analog output path thus provides a full scale peak-to-peak differential AC output voltage of approximately 1.75v p-p when the outputs are terminated with high impedance.

While this level is sufficient to drive most AQM devices beyond their linear operating region, it may be desirable in some applications to increase or decrease the full-scale output levels in order to maximize dynamic range of the path. The full-scale output level can be modified by changing the DAC current setting resistor, R9, to raise or lower the full-scale DAC current. The maximum DAC current is 20 mA, which would result in a maximum possible full scale output voltage of approximately 2.25 v p-p.

Lower output levels can be achieved also by attenuating the digital signal in the ISL5239 ahead of the DAC. But if full dynamic range is desired at full-scale levels substantially below 1.75 v p-p, then we advise reducing the full-scale DAC current range by changing R9.

Changing the DAC current scale will also effect the DC bias voltage at the DAC outputs and may require also changing the common mode biasing resistor so as to restore a mid-point bias voltage near the 0.35 vdc level. These types of changes, if needed, should be performed by an experienced analog circuit designer.

The full-scale output signal voltages can be adjusted over a reasonably wide range without significant loss of dynamic range by using only the digital level scaling capabilities of the ISL5239.

Output Loading

In typical applications, the analog I and Q outputs will be connected to relatively high impedance loads (e.g. AQM inputs) through short low-capacitance coax cables, preferably less than 6 inches. In this configuration, the coax lines are singly terminated with source series terminations of 50Ω.

A short length will ensure that the pole frequency of the 50Ω output impedance of the drivers, when combined with loading capacitance, will have a corner frequency beyond 200 to 300 MHz.

Longer coax connections can be used if the outputs are either doubly terminated or divided through a higher value resistor into a 50Ω terminated line.

The high frequency distortion performance of the AD8138 buffer amplifier depends on the output loading. For best performance the total loading, including 50Ω series termination resistor should be greater than 300Ω.

Since output loads will likely be coupled at DC, the common mode DC output bias voltage may result in DC current sourced to the load. The combination of low output load resistance and high common mode voltage will shift the output bias of the AD8138, causing some degradation in distortion performance. Thus, we recommend keeping the load resistances high (greater than a few hundred ohms) when using significant amounts of common mode DC bias.

Optimum loading conditions are easily satisfied when the ISL5239 Evaluation Board is driving an AQM RFIC device over short coax cables.

The +ve and -ve analog outputs may be loaded differently without effecting the balanced differential characteristics of the low pass filters.

Typical Performance

In this section, we show examples of typical measured performance of the ISL5239 Evaluation Board analog output signals, when driving the Sirenza STQ-2016 RF quadrature upconverter Eval Board. The Sirenza Eval Board has been modified to place 20Ω series resistors in the differential input paths in place of capacitors to enable DC-coupled drive.

Short equal length 50Ω coax cables were used to interface the ISL5239 Eval Board to the Sirenza Eval Board. The DC common mode output voltage was adjusted to 1.90 vdc. The Sirenza Eval Board is set-up to perform direct upconversion to a carrier center of 2.14 GHz.

Upconverted Signal Spectrum

The spectrum analyzer plot below shows the resulting RF output with a properly adjusted output. The path is comprised with a cascade of 4 - ISL5217 Digital Upconverter Eval Boards driving the ISL5239 Eval Board, in turn driving the Sirenza STQ-2016 Analog Quadrature Upconverter Eval Board.

Each ISL5217 Board is producing one of the four wideband CDMA carriers shown in the spectrum. The total occupied bandwidth of the signals is 20 MHz.

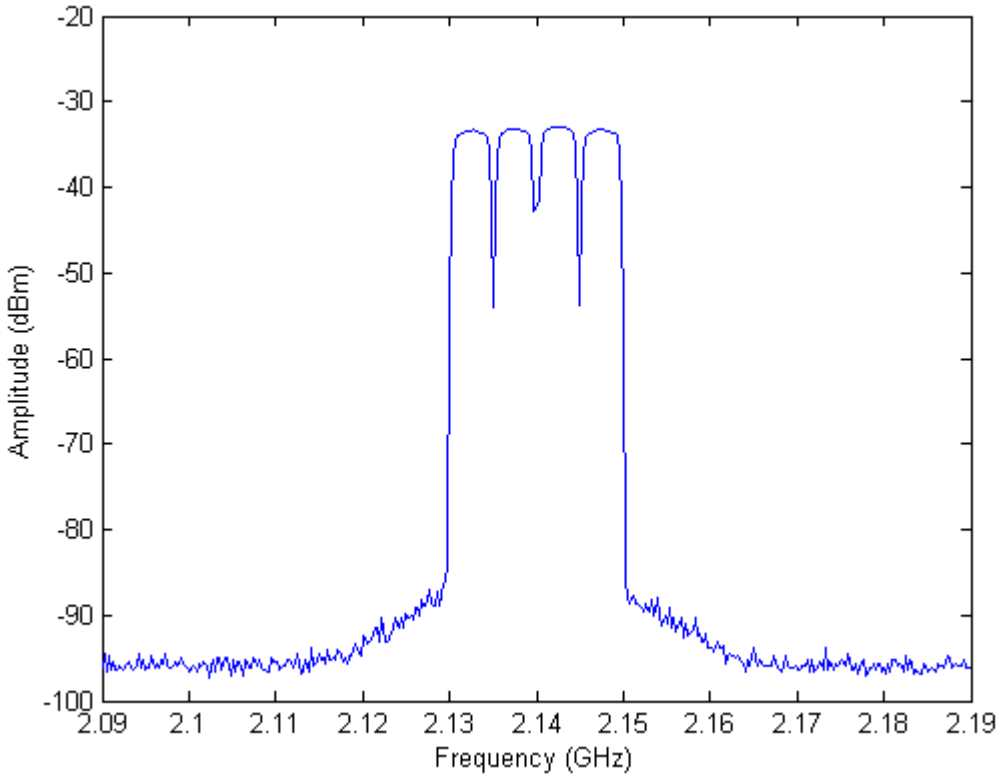

FIGURE 11. MEASURED OUTPUT OF THE EVAL BOARD AND UPCONVERTER

Resolution and video bandwidths are 3kHz and 1 kHz respectively.

The small of residual distortion indicated in this measurement is due to roughly equal distortion contributions of the STQ-2016 upconverter and the spectrum analyzer. The baseband signal (not shown) exhibits only analyzer distortion and has a signal-to-noise ratio of about 70 dB. The dynamic range limitation of approximately 65 dB shown here at RF is due to the upconverter RFIC and analyzer noise floor limits.

In achieving full dynamic range performance, it is important that the combined digital output signal levels be adjusted through the signal path in order to utilize nearly the full dynamic range of the DAC outputs and analog outputs. If the signal level is lowered, the analog noise floor of the upconverter will remain at the same level, reducing the RF output signal-to-noise ratio.

The sampling image spectrum at 125 MHz offset is limited by a combination of DAC sinc rolloff and analog low pass filter characteristics.

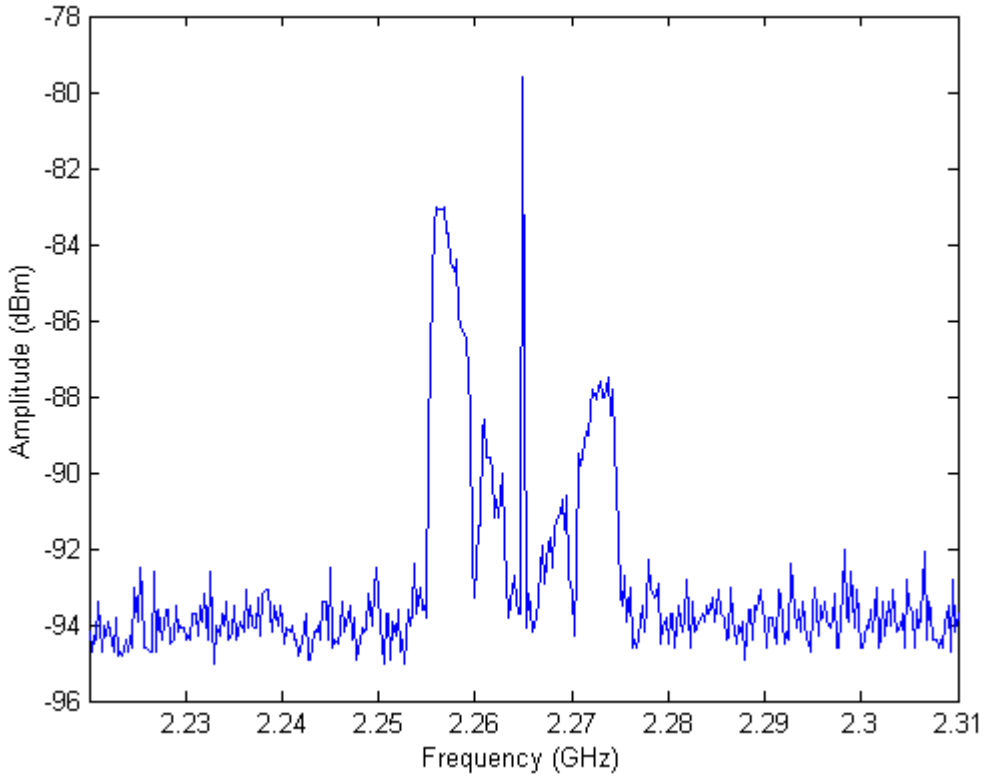

FIGURE 12. MEASURED OUTPUT AT 125 MHz OFFSET (SAMPLING IMAGE)

The spectrum analyzer plot below shows the measured spectrum corresponding to the above signal, centered at 125 MHz offset, or equivalently 2.265 GHz.

This spectrum, shown with vertical scale of 2 dB per division, shows the relative levels of the clock feedthrough signal at 2.265 GHz and the filtered image spectrum due to DAC sampling.

The 125MHz clock feedthrough is shown at -79.5 dBm. Total signal power is approximately +4.5 dBm, equating to a clock feedthrough power level of -84 dBc.

The plot shows that the DAC sampling spectral image is approximately -50 dBc at the lower corner of the spectrum, corresponding to 115 MHz offset at baseband.

Other than the clock feedthrough component, the spectrum is void of any significant spurs when detected in a 3 kHz resolution bandwidth scan.

Passband Frequency Response

The frequency response characteristics of the cascade ISL5239 Evaluation Board/Sirenza

STQ-2016 AQM Eval Board were measured by outputting a digitally generated wideband pulse signal with ideally flat spectrum over 100 MHz bandwidth.

The resulting spectral output is shown below.

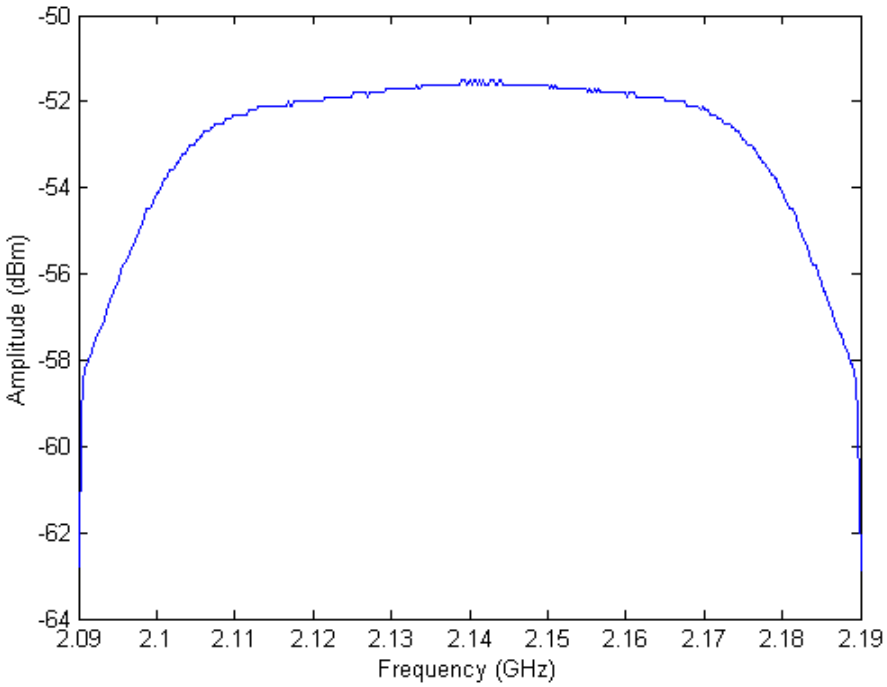

FIGURE 13. MEASURED SPECTRAL RESPONSE OF THE EVAL BOARD AND UPCONVERTER

The vertical scale is again 2 dB per division. The plot shows approximately 4.0 dB rolloff at frequencies of +/-42 MHz from center. Taking into account the sinc(x) response rolloff of the DAC, the rolloff contribution due to the analog output path filters is approximately 2.4 dB.

The measurement shows that the 3 dB corner frequency response of the analog path is slightly above 42 MHz, as expected.

Response Equalization Using ISL5239 Correction Filters

Measured data presented above was obtained with the digital correction filters of the ISL5239 disabled.

In pre-distortion applications, the correction filters should be employed to equalize the response of the baseband analog channel.

With the version-1 low-pass filters that are shipped with the ISL5239 Evaluation Board, the correction filters will equalize the passband response over 80 MHz to 85 MHz bandwidth to well within 0.1 dB flatness.

To obtain an equivalent flat response over 100 MHz of bandwidth, version-2 or version-3 low-pass filter modifications should be used, as described in this App Note.

The digital correction filters can also be used to equalize magnitude and delay differences between the I and Q channels in order to obtain nearly ideal image response over these bandwidths. This topic is covered in other Application Notes for the ISL5239.